Evaluating the Impact of STI Recess Profile Control on Advanced FinFET Device Performance

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Abstract

In this paper, a 5 nm FinFET flow was built using the SEMulator3D® virtual fabrication platform. Different STI (shallow trench isolation) recess profiles were investigated using the pattern-dependent etch capabilities of SEMulator3D, including changes in trenching/footing profile, fin height and imbalance fin height. The impact of STI recess profile on device performance was then investigated using a built-in drift-diffusion solver. Our analysis has confirmed that larger footings, lower fin heights and larger imbalance fin heights will generate more severe DIBL problems and lead to higher off-state leakage. STI recess with an optimal trenching profile can increase on-state current and reduce off-state leakage. (Keywords: 5 nm, FinFET, STI recess profile, virtual fabrication, device simulation)

Introduction

With semiconductor devices scaling to the lowest achievable limits, micro loading and device structure variability have become key factors in device performance [1]. In FinFET devices, effective channel width is a function of the fin reveal height established during the STI recess process. Studying the impact of STI recess profile changes on FinFET performance is a meaningful exercise, since it guides device variation control and process optimization.

Traditionally, it is difficult to perform a variation split experiment, such as an STI recess profile split, directly on a Si wafer since variation can differ among structures built under the same process conditions. Also, cycle time for these variation experiments is long, and the cost of silicon experimentation is high, especially when studying a FEOL (front end of line) split and having to collect the results after BEOL (back end of line) electrical testing. Under these circumstances, virtual fabrication can save both time and money [2].

In this paper, different STI recess profiles were investigated using a TechInsights® teardown design for a 7 nm node FinFET chip. SEMulator3D virtual fabrication was used to build a full loop 5 nm FinFET flow (along with various STI recess profiles) using pattern dependent etch modeling. An integrated drift-diffusion solver was then used to study the impact of STI profile variations on device performance.

STI Profile Investigation and Realization

A. STI Profile Investigation

This study of STI recess profiles was started by modeling multiple structures in a 7 nm logic chip. 3 common phenomena were identified, including STI footing issues, STI imbalance and fin height variation (Figure 1) [3]. STI footing problems are usually caused by STI CMP dishing and local etch rate loading during the fin recess process. Fin height variations and imbalance can occur due to pattern density loading among different structures.

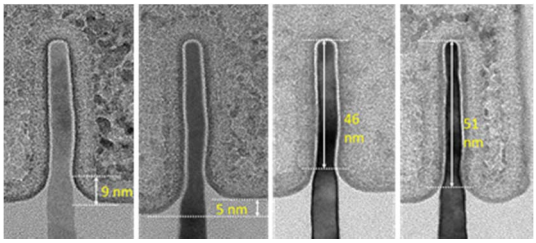

Fig. 1: STI recess profile of an 7nm logic chip (Courtesy: TechInsights).

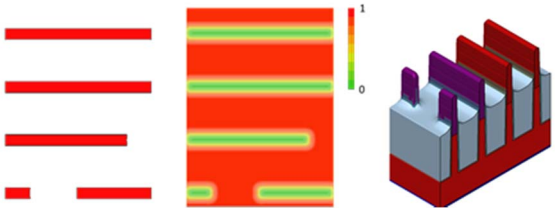

Fig. 2: Pattern dependent mask, 2D loading map and 3D loading structures.

B. STI Profile Studies Using Virtual Fabrication

SEMulator3D provides a novel pseudo-3D approach to pattern dependence modeling based upon 2D proximity functions. The proximity functions are convoluted using a pattern-dependence mask, within a characteristic distance of a point of interest, and can subsequently yield a 2D loading map. This 2D loading map modifies the behavior of a 3D behavioral etch algorithm in the software [4]. In our study, a 5 nm SRAM111 fin pattern was modeled using a pattern dependent mask. After proper configuration of the pattern-dependence parameters, a 2D etch rate loading map was generated. Next, a virtual 3D STI footing structure was created using this loading map (Figure 2). Using a combination of fin height and pattern dependence variations in a virtual split

experiment, we realized STI footing/trenching, fin height imbalance and fin height profiles using the virtual fabrication platform (See Fig. 3).

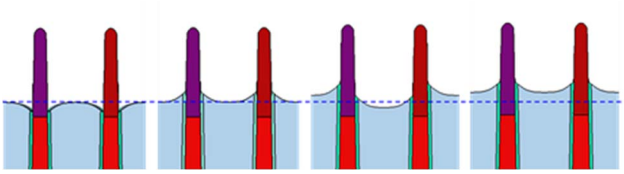

Fig. 3: Different STI recess profiles generated in the virtual fabrication platform.

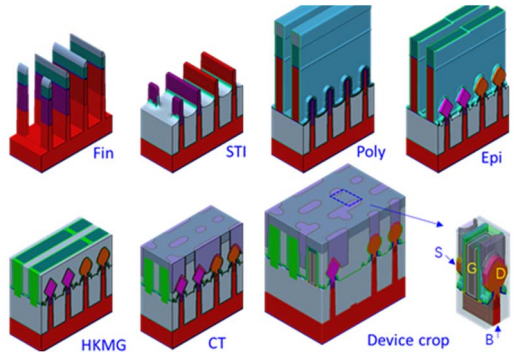

Fig. 4: 5nm FinFET main process steps.

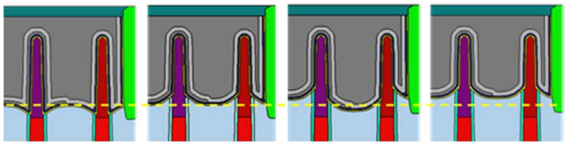

Fig. 5: Final STI recess profile

Table 1: Split table.

No.	FinH/nm	Footing/nm	Imbalance/nm
R1	50	-15.5	0
R2		-6	
R3		0	
R4		7	
R5		15	
R6	45	7	
R7	55		
R8	50		8
R9			12

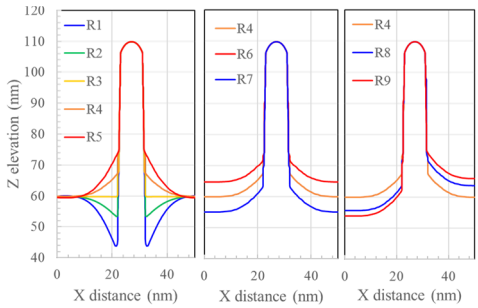

Fig. 6: STI profiles of different split conditions.

Flow Build Up and Device Simulation

A. Flow Build Up Under Split Conditions

To evaluate the impact of the STI recess profile on device performance, a full loop 5 nm FinFET process flow from the fin to the contact was built using SEMulator3D. In this flow, SRAM111 was selected as the nominal structure, with a fin CD of 6 nm, a fin height of 50 nm, a source/drain Si recess depth of 45 nm, a source/drain doping concentration of 10^{19} & 10^{20} cm^{-3} for the seed and bulk layers, along with a well implant concentration of about $1e^{18}$ cm^{-3}. Finally, an NMOS structure was cropped out for device simulation (See Fig. 4). During STI recess, different STI recess profiles were generated for testing. Figure 5 displays the final profiles after contact wire looping. During our STI footing/trenching, fin height and fin height imbalance study, 9 simulation trials were completed under the split conditions shown in Table 1. Fig. 6 lists the corresponding elevation profiles generated under these split conditions.

B. Device Simulation and Analysis

Next, an electrical device simulation was performed using a drain voltage of 0.8 V, and a gate voltage sweep from 0 to 1 V (with steps of 0.05 V). Figure 7 highlights the I_D-V_G curve in both linear and log scales for different split conditions. Figure 8 reveals the off-state leakage status across the chosen drain voltage sweep range. Larger footings and lower fin heights exhibit much higher off-state leakage and slightly lower on-current. These problems were not readily seen during changes in fin height imbalance. From the leakage curve, it is obvious that higher leakage is caused by increased DIBL effects seen with lower fin heights and larger footings. The leakage current distribution was also visualized using the SEMulator3D modeling platform (see Figure 9). The main contributing factor to leakage current appeared to be source drain punch through at the fin bottom. Fig. 10 displays a summary of major electrical performance parameters in the different split experiments. ID_SAT, IOFF_SAT, VT_SAT, Subthreshold swing, DIBL and Gate to Source/Drain capacitance simulation results are shown. A clearly quantified relationship can be seen among the varied split conditions. The V_T shift is within a 10 mV range among each of the simulation runs. Devices with a deeper trenching profile and higher fin height displayed a much higher on-state current and lower off-leakage. This is mainly due to a larger effective channel width and good gate control at the fin bottom, which can also be seen looking at the subthreshold swing and DIBL results of this split.

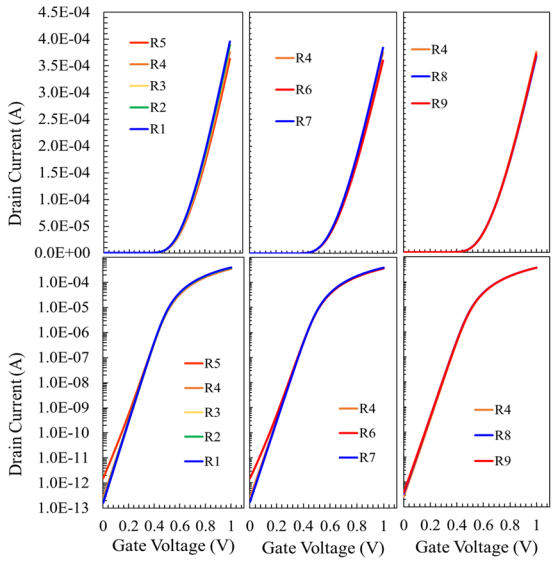

Fig. 7: ID-VG curve of different splits.

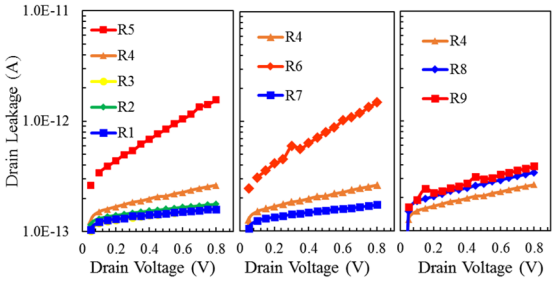

Fig. 8: Drain leakage with drain voltage sweep.

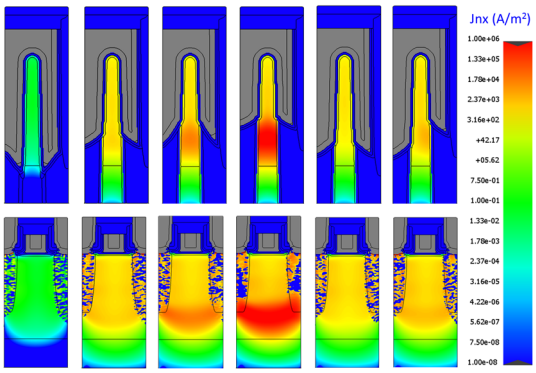

Fig. 9: Leakage current distribution from different directions.

Based upon these results, we can see that both STI footing issues and imbalanced fin heights can lead to diminished gate control at the fin bottom, similar to the issues seen at a lower fin height. To overcome this problem, an optimal trenching STI profile can be designed which can both boost on-current conditions and lower off-leakage current. The difficulty in using a trenching profile is that it requires very good control of poly etch processes, to avoid poly residue in the trench. In addition, the trenching profile also introduces a slightly higher capacitance between the gate and the source/drain. If footing, imbalanced fin heights and lower fin height issues need to be addressed, either implantation or using an SOI structure at the fin bottom may be required to avoid source-drain punch through and higher leakage.

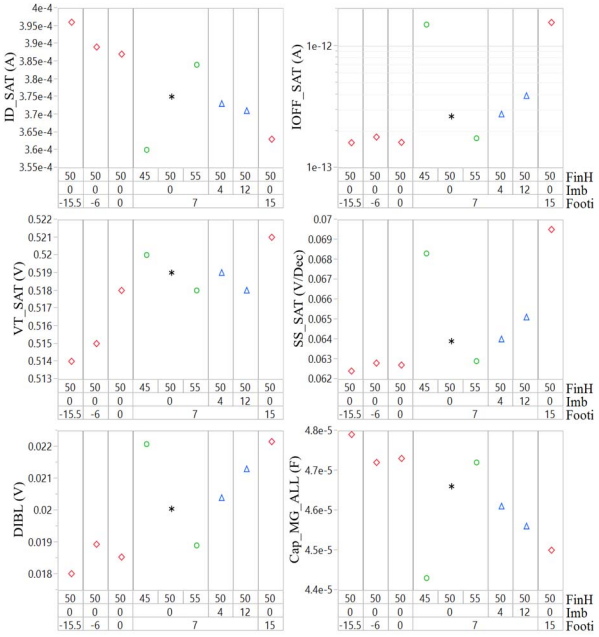

Fig. 10: A summary of major electrical performance.

Conclusion

In this study, STI recess profiles for a 5 nm FinFET process were studied using virtual fabrication. We discovered that STI recesses with a trenching profile can improve on-state current and lower off-state leakage, while footing and imbalance fin issues can exacerbate leakage under certain conditions. In our simulation studies, the leakage path occurred at the fin bottom, where the source/drain and gate electrical fields compete with each other to control the space charge. These results demonstrate that rigorous STI profile control may be required to meet performance specifications in an advanced FinFET process setting.

References

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